IN THE CLAIMS:

1. (Currently Amended) A latch comprising:

a clocked trans-admittance stage circuit for ~~receiving a voltage and~~ producing a current output responsive to an input voltage; and

an active load connected to receive input data and said current output as input ~~the current output of said trans-admittance circuit~~ and produce a voltage output that is received by said clocked trans-admittance stage circuit to control at least one element thereof to provide a data output.

2. (Original) The latch in accordance with claim 1, wherein the active load is a trans-impedance stage circuit.

3. (Original) The latch in accordance with claim 1, wherein said trans-admittance stage circuit comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

4. (Previously Presented) The latch in accordance with claim 3, wherein the base of said first and second transistors are clocked on opposite phases of a clock signal.

5. (Original) The latch in accordance with claim 4, wherein the base of said third transistor receives as input a voltage signal and the base of said fourth transistor receives as input an inverted voltage signal, said third transistor produces a current output signal based on the inverted voltage signal, and said fourth transistor produces an inverted current output signal based on the voltage signal.

6. (Original) The latch in accordance with claim 1, further comprising transmission lines coupled between said clocked trans-admittance circuit and said active load.

7. (Currently Amended) A cascaded latch chain comprising:

a clocked trans-admittance stage latch configured to ~~receive an input voltage and~~ produce an output current responsive to an input voltage; and

at least one latch pair configured ~~connected~~ to receive an input data and the output current and provide a voltage output to control at least one element of said clocked trans-admittance stage latch to provide a data output ~~thereof and produce an additional output current~~.

8. (Previously Presented) The cascaded latch chain in accordance with claim 7, wherein said at least one latch pair includes two combined trans-admittance and additional trans-impedance stages.

9. (Previously Presented) The cascaded latch chain in accordance with claim 8, comprising at least two latch pairs including a first latch pair and a last latch pair, each latch pair having two trans-admittance and trans-impedance stages, the two trans-admittance and trans-impedance stages of each latch pair being clocked on opposite phases of a clock signal.

10. (Original) The cascaded latch chain in accordance with claim 9, wherein said trans-admittance stage in each latch pair comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors; a

second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

11. (Original) The cascaded latch chain in accordance with claim 9, wherein the two trans-admittance and trans-impedance stages in said at least one latch pair are clocked on opposite phases of a clock signal.

12. (Previously Presented) The cascaded latch chain in accordance with claim 7, further comprising a trans impedance stage latch connected to receive the output current of a final latch pair and produce an output voltage.

13. (Previously Presented) The cascaded latch chain in accordance with claim 8, further comprising a trans impedance stage latch connected to receive the output current of a final latch pair and produce an output voltage.

14. (Currently Amended) A latch pair comprising:

a first combined trans-admittance and trans-impedance stage coupled to an independently clocked second combined trans-admittance and trans-impedance stage, wherein each of said first and said second combined stages have an input and an output, and at least one of said combined

trans-admittance and trans-impedance stages has a clocked trans-admittance stage circuit for producing a current output responsive to an input voltage; and

an active load configured to receive input data and said current output and produce a voltage output that is received by said clocked trans-admittance stage circuit to control at least one element thereof to provide a data output.

15. (Previously Presented) The latch pair in accordance with claim 14, wherein each trans-admittance stage of said first and said second combined stages comprises:

a first pair of transistors including a first transistor and a second transistor, the first and second transistors each having a base, an emitter, and a collector;

a current source connected to the emitter of each of said first and second transistors;

a second pair of transistors including a third transistor and a fourth transistor, each of said third and fourth transistors having a base, an emitter, and a collector; and the emitter of each of said third and fourth transistors being connected to the collector of said first transistor; and

a third pair of transistors including a fifth transistor and a sixth transistor, each of said fifth and sixth transistors having a base, an emitter, and a collector; and the emitter of each of said fifth and sixth transistors being connected to the collector of said second transistor.

16. (Previously Presented) The latch pair in accordance with claim 14, wherein said first and said second combined stages are clocked on opposite phases of a clock signal.

17. (Canceled)

18. (Previously Presented) The latch pair in accordance with claim 14 wherein trans-admittance stages of said first and said second combined stages have transistors with collectors that lack a common coupling point.

19. (Previously Presented) The latch pair in accordance with claim 14 wherein transistors of a trans-admittance stage of said first combined stage have collectors directly coupled to said input and said output of said first combined stage.

20. (Previously Presented) The latch in accordance with claim 1 wherein said active load is coupled to Vcc.